REVISTA FCEFyN

WNOCs-LNA Development Feasibility: A study using free software tools and predictive models

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Abstract— Wireless networks on chips allow solving, among others, the problems associated with the use of wired buses. Current works show that they are also very suitable to achieve characteristics such as performance, reliability and graceful degradation scalability. This work demonstrates the development feasibility of one of the required radio frequency modules, using free tools and models. In particular it is shown that it is possible to meet a set of basic requirements for a wireless network on chip low noise amplifier . It is also shown that the freely available predictive models, allow to extend the operating frequencies and anticipate even more demanding future requirements. As a consequence, these wireless micro networks are emerging as a fundamental building block in the development of future robust systems, such as segmented architectures, driver-less vehicles and autonomous bio-medical equipment.

Keywords— Wireless, Networks, Chips, feasibility, amplifiers, predictive, models, free, software, robust, systems.

Resumen— Las redes inalámbricas en circuitos integrados permiten solucionar, entre otros, los problemas asociados al uso de múltiples cables de interconexión. Trabajos actuales muestran que además resultan muy adecuadas para lograr características tales como la escalabilidad en la performance, la confiabilidad y el deterioro paulatino. Este trabajo demuestra la factibilidad del desarrollo, mediante herramientas y modelos libres, de uno de los módulos de radio frecuencia necesarios. En particular se demuestra que es posible cumplir con el conjunto de requerimientos básicos de un amplificador de bajo ruido para estas micro redes inalámbricas. Se muestra también que los modelos predictivos disponibles de forma libre, permiten extender las frecuencias de operación y anticiparse a futuros requerimientos aún más exigentes. Como concecuencia, estas micro redes inalámbricas se perfilan como una pieza constructiva fundamental en el desarrollo de futuros sistemas robustos, tales como arquitecturas segmentadas, automóviles sin conductor y equipamieto bio-médico autónomo.

Palabras clave— inalámbricos, redes, circuitos integrados, factibilidad, amplificadores, predictivos, modelos, libre, software, robustos, sistemas.

INTRODUCTION

High Performance Computing *(HPC)* is an increasing demand in current and future critical systems (Barnell et al., 2018). This is due to the growing use of computing intensive techniques such as machine learning, and complex routing algorithms in Internet of Things *(IoT)*, among other reasons (Nengzhi et al., 2020). HPC strongly benefits with the use of multi processors systems *(MPS)*, (Bryant and O'Hallaron, 2016). Traditionally, MPS are implemented in System On Chips *(SOCs)* with various processors interconnected by means of wired buses, (Zhang et al., 2010). This buses in general use cross-bars or switches to implement a certain network topology. As transistors sizes and voltages diminish and the operation frequencies increased with each technology improvement, the wired buses became gradually a performance bottleneck. This is mainly due to power consumption associated with high frequency transistor switching and wire caused delays. In this context, wireless packet-switched networks inside a chip became an appealing alternative (Zhao et al., 2015). In fact Wireless Network on Chips *(WNOCs)* are becoming an active field of research and development, (Poovendran et al., 2019). Although optical communications is the most desired communication media, there are still many technological challenges that need to be solved before its use in WNOCs, (see for example (Wikipedia, 2021) and (Wang et al., 2021)), specially with free tools

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and models. On the other hand, radio frequency *(RF)* technology in the required frequencies is mature and currently a more feasible way to implement WNOCs. Future critical systems will not only demand high performance, obviously they will also demand high reliability and availability, i.e. dependability. Traditional ways to achieve high dependability make MPS-SOCs very expensive and un-scalable. Performance and Dependability Scalability *(PDS)* together with graceful degradation are also key desired characteristics of some of the future critical systems. Current works show that all these properties are naturally present in WNOCs (Matolak et al., 2012). However, it is necessary to carefully study the feasibility aspects of WNOCs before starting a complete development effort. More precisely, it is necessary to study if WNOCs can be developed in a cost-effective manner, prior to their development for a particular or for a general purpose. This work focus on the development-feasibility of one of the required WNOCs RF modules. More specifically, it shows the development-feasibility of a Low Noise Amplifier *(LNA)*. LNA is a fundamental piece in the WNOCs transceivers, and its development indicates that the other required RF modules can also be developed with the same tools and models. In the next section wired and wireless networks on chips are revised ending with a set of possible radio frequency ranges that could be used in current developments. With that set of previously selected frequency ranges in hand, the following section named *("Low Frequency" LNA)*, shows the feasibility of implementing a typical 2.4 GHz LNA with free software tools and models. Since the expected behaviour of these LNAs is well known, the tools and models are also validated giving a strong fulcrum to proceed forward.The next section, named *("High Frequency" LNA)*, explores the development of a 50 GHz amplifier using predictive models. The last sections relates the previous steps with future ones showing that WNOCs are completely feasible to be developed using free software tools and models. This last section strongly supports the rationale of using WNOCs as a basic building block in future critical systems, such as such as segmented architectures, driver-less vehicles and autonomous bio-medical equipment.

NETWORKS ON CHIPS

As previously stated, Networks on chips could help in solving many of the problems associated with wired interconnection buses and promise a high degree of scalability on various system's desired properties. They can be implemented in a wired or in a wireless fashion.

Wired Networks on Chips

Wired Networks on Chips or simply *(NOCs)* are composed of the following main elements:

- Processing Element (PE): Each PE module, generally contains one or more processors.
- Router (R): Handles communications between different PEs. Each router is associated to a single PE.
- Link: Physical connection between Routers, wires, in this case.

The set PE + R is called *Node*. As shown in Fig. 1, there are many possible topologies for NOCs. Some of the most common are: *Meshes*, *Rings* and *Torus* (Pasricha and Dutt, 2008).

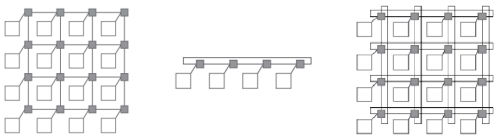

Fig. 1: Common NOCs topologies: Mesh, Ring and Torus. Squares represent PEs, small black circles, represent Routers. Solid lines represent wired physical links

Wireless Networks On Chips

Although relatively small wired networks on chips, *(NOCs)*, can help in solving performance and power dissipation problems, they cannot scale very easily for large number of nodes. On the other hand, Wireless Networks On Chips *(WNOCs)* are a natural environment for scalability. More over, recent works show that WNOCs can make easier the implementation of Wireless Networks Between Chips *(WNBCs)*, Wireless Networks Between Boards *(WNBBs)*, and so on. Multiple point to multiple point RF wireless communication, could happen at the same time, with proper Media Access Control *(MAC)* schemes. The main contribution of this work is to determine the development feasibility of one of the RF modules required for WNOCs implementations. Available research show that in the RF band that ranges from 50 to 150 GHz the required RF modules can be implemented in nowadays availalbe CMOS micro electronic technologies with reasonable area and power consumption (Matolak et al., 2012). However, the required micro antennas and inductors may suffer from near field and cross-coupled interference. Those problems can be better tackled in the 150 to 500 GHz band, but the required technology is SiGe-BiCMOS, which is less appealing from the implementation perspective. Problems associated with antennas and inductors may be overcome using even higher frequencies such as the 500 GHz to 3 THz range and even better with optical communications inside the chip. However the required micro electronic technology is still immature or unavailable in the free software tools ecosystem. As a consequence, the current RF frequency ranges that are currently candidates for WNOCs are listed in Table 1, In fact, Table 1 can be viewed as a first step or result in determining the feasibility of the required WNOCs-RF-modules. This result is justified based on the previous trade-off analysis. The second step is discussed in the next section.

TABLE 1: CURRENT WNOCS RADIO FREQUENCY FEASIBILITY

	Frequency Ranges		
	50 to 150 GHz	150 to 500 GHz	500 GHz to 3 THz
Feasibility Level	High	Medium	Low

"Low Frequency" LNA

From Table 1 it is clear that it is convenient to select the 50 to 150 GHz frequency range for this first study. The second step that is taken in this work conists in selecting a "low frequency" for a first LNA implementation. The first operation frequency selected was 2.4 GHz. The rationale of doing so, relies on the following facts:

- 2.4 GHz LNAs behaviour is well known and described in many current and previous published works.
- Current CMOS technology has already been tested with commercial software tools and models in the 2.4 GHz frequency range and in higher frequencies.

As the first stage on the Rx block of a receiver, the LNA must achieve a series of requirements, such as gain, linearity, stability, among others; However, the most important LNA requirement is its Noise-Figure *(NF)* (see ec. (1)). It is important to keep *NF* as low as possible, since its noise contribution will be the most decisive in determining the whole receiver's *NF* (Lee, 2003).

$$NF = 10 * log(\frac{SNR_{in}}{SNR_{out}}) \quad (1)$$

The proposed basic requirements set for the 2.4 GHz are listed in Table 2. They were selected on the basis of the same parameters published for other 2.4 GHz LNAs.

Table 2: 2.4 GHz LNA requirements.

Parameter	Value
Operation Frequency fo	$2{,}4GHz$
Noise Figure	$2dB$
Gain	$15dB$
Linearity IIP3	$-7dBm$
Stability	*Absolute*
Power consumption	$5mW$

Efabless

This first *"low frequency" LNA* was designed within the Efabless free software tools ecosystem, (efabless, 2021a). Efabless is an online platform for innovation and design of Intellectual Property Cores *(IPC)* that allows its users to design certified circuits and get them to *Tape-Out*, i.e. to fabricate the chips, at a low cost through the open multiple project wafer shuttle program *(MPW)*, (efabless, 2021b). It's a continuously growing environment with designers from all over the world, and turns out to be a solid option for fab-less companies, designers, or even students to accomplish competent designs in the integrated circuits marketplace. This platform provides, at least, two software tools for analog design and validation: Electric VLSI as the schematic tool, and Magic VLSI as layout tool. It also provides, currently, two official technology process from XFAB: 180nm and 350nm. It is very important to note that efabless, together with Skywater (Skywater, 2021) and Google are supporting the Open MPW program. This program requires that the developments should be open source and free. However, for commercial purposes developments, the ChipIgnite program allows the development of integrated circuits within a very low cost process. The existence of these two options clearly enables the developments at zero or very low cost.

2.4 GHz LNA Topology

The transistor model used for this 2.4 GHz LNA is XFAB 180 nm, one of the two technologies available in the Efabless platform. The LNA was designed in a cascode topology with inductive degeneration. This topology provides low noise, good gain and linearity, and good overall performance with narrow band response (NXP, 2013). Both input and output networks were matched to 50 ohm using matching networks. The final schematic design is shown in Fig. 2.

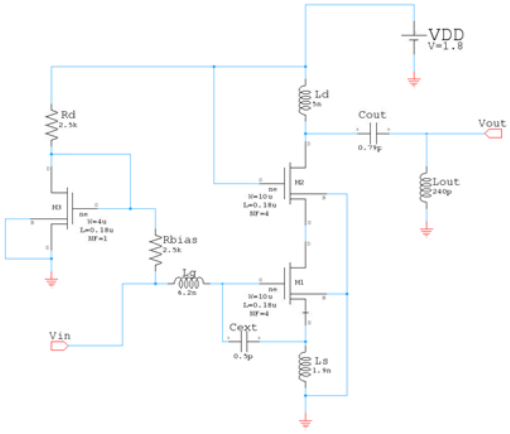

Fig. 2: 2.4 GHz LNA schematic design

Simulation Results

The simulation results are shown in Table 3. Some of the *"low frequency" LNA* simulation results overcome the expected values proposed in Table 2, showing a Noise Figure of 1,1dB and 24,7 dB of Gain; However the power consumption, exceeds the required value by 20%. Since this work objective is just to study the feasibility of design, the results are considered to be acceptable, with the possibility to be improved in future works.

Table 3: 2.4 GHz LNA simulation results

Parameter	Requirements	Simulation Results
Operation Frequency fo	$2{,}4GHz$	$2{,}4GHz$
Noise Figure	$2dB$	$1{,}1dB$
Gain	$15dB$	$24{,}7dB$
Linearity IIP3	$-7dBm$	$-2{,}14dBm$
Stability	*Absolute*	*Absolute*
Power consumption	$5mW$	$6{,}12mW$

Layout Results

The corresponding layout design is shown Fig. 3, meeting Design Rules Checking (DRC) and Layout Vs Schematic (LVS) checking. The total pad area is 460um * 500um. At higher frequencies, it is expected that required area is smaller. The next step in this feasibility study is described in the next section.

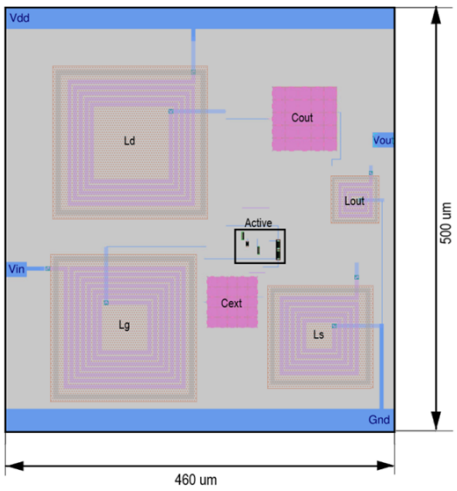

Fig. 3: 2.4 GHz LNA layout design

"High Frequency" LNA

The third step that was taken in order to determine WNOCs-LNA development-feasibility, was to develop a 50 GHz LNA. This second LNA was designed to achieve a new set of requirements, up scaling the operation frequency of the previous amplifier. This was achieved using LTspice as the schematic design tool, and the selected transistor model is PTM 45 nm from Predictive Models. Though there are more modern technologies available, like 7nm, the 45nm technology was chosen in order to increase the possibility to access a tape out in a similar technology process in the near future. As seen in Table 4, the 50 GHz LNA requirements are similar to those of the 2.4 GHz LNA, except of course the center band frequency.

Table 4: 50 GHz LNA requirements.

Parameter	Value
Operation Frequency fo	$50{,}0GHz$
Noise Figure	$2dB$
Gain	$15dB$
Linearity IIP3	$-7dBm$
Stability	*Absolute*
Power consumption	$5mW$

50 GHz LNA Topology

Similarly to the 2.4 GHz amplifier, this LNA was designed in cascode topology with inductive degeneration, and both input and output impedance matched to 50 ohm. The final schematic is shown in Fig. 4.

Simulation Results

The simulation results shown in Table 5. It's important to note that achieving similar results at such a higher frequency is not a simple task, therefore some requirements are not met, mainly Power Consumption and Gain. However, again, these results are not seen as bad and could be improved in future works.

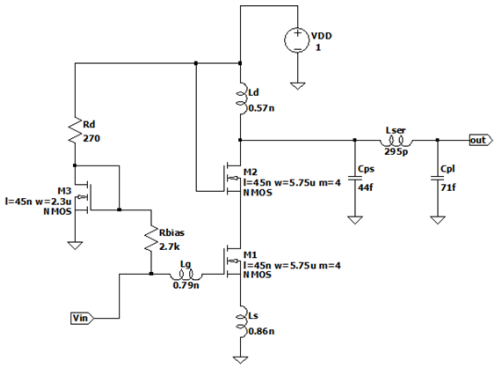

Fig. 4: 50 GHz LNA schematic design

Table 5: 50 GHz LNA simulation results

Parameter	Requirements	Simulation Results
Operation Frequency fo	$50Hz$	$50GHz$
Noise Figure	$2dB$	$2{,}01dB$
Gain	$15dB$	$9{,}77dB$
Linearity IIP3	$-7dBm$	$-0{,}7dBm$
Stability	*Absolute*	*Absolute*
Power consumption	$5mW$	$11{,}2mW$

Predictive Models

Predictive Models is a set of CMOS technology processes developed by the university of Berkeley that aims to resemble the latest technology processes from official FABs, being completely free for academic usage. Although these are not real models that could be used for a tape-out, they allow designers to anticipate results if an official process were available, or even study the results of future processes not yet developed. It offers a wide variety of models ranging from 350nm to 7nm.

Layout Results

Since these predictive models do not include the layout process information, no layout was designed at this step. However, as previously stated, it is highly feasible that official process will soon be available for very similar technologies.

Conclusions and Future Work

In this work the first steps were taken to demonstrate WNOCs-LNA Development Feasibility using free software tools and predictive models:

In the first step, the suitable frequency ranges for the internal RF links were identified. A brief cost-benefit analysis was presented for each possible band.

In the second step, a subset of the free software tools available for model-level simulation and layout-level simulation were validated. To do that a 2.4 GHz LNA was completely developed and verified with that tools. The results where compatible with previous similar publications such as (Martínez-Pérez et al., 2019), (Martinez-Perez et al., 2020), (Asharani and Nagabhushan, 2018), showing a complete agreement and achieving the desired tool validation.

The third step used predictive models to demonstrate that a 50 GHz LNA can also be simulated with free software tools at the model level. Since the required PDK for these models is still not available, layout simulations were not performed.

Recently, free PDKs compatible with the previous predictive models are becoming available through efabless, skywater and Google. Hence, WNOCs-LNA Development Feasibility using free software tools and predictive models have been demonstrated.

Our next steps include the following ones:

Achieve the layouts simulations at 50 GHz and higher frequencies, in order to enable the tape-out of a SOC, implementing a WNOCs, vía the MPW and efabless ecosystems.

Achieve the layouts simulations of other RF modules such as mixers, down converters, filters, etc., in order to complete a WNOCs RF transceiver.

Another important task to be initiated in the near future, will be the development of an optical WNOC transceiver for intra-chip communications.

Of course all this developments are planned with the use of free software tools, free models and free tape-out facilities.

In this way we are opening a complete new dimension in the development of all kind of current and future robust systems, giving an important step in state of the art in this area.

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